## AMENDMENTS TO THE CLAIMS

Claims 1-19 (Cancelled)

20. (New) A semiconductor device comprising:

a semiconductor chip;

at least a first electrode formed on a first major surface of said semiconductor chip;

at least a second electrode formed on a second major surface of said semiconductor chip opposite to said first major surface; and

at least a conductive member connecting said first electrode to said second electrode and covering a side surface of said semiconductor chip.

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21. (New) The semiconductor device according to claim 20, wherein the second major surface is formed of an insulating layer.

22. (New) The semiconductor device according to claim 20, further comprising a conductive line pattern extending from said second electrode.

23. (New) A composite semiconductor device structure, comprising at least two semiconductor devices as defined in claim 20, wherein

said at least two semiconductor devices are stacked on each other, and

a conductive member of a lower one of said semiconductor devices is connected to a conductive member of an upper one of said semiconductor devices.

24. (New) A composite semiconductor device structure, comprising at least two semiconductor devices as defined in claim 21, wherein

said at least two semiconductor devices are stacked on each other, and

a conductive member of a lower one of said semiconductor devices is connected to a conductive member of an upper one of said semiconductor devices.

25. (New) A composite semiconductor device structure, comprising at least two semiconductor devices as defined in claim 22, wherein

said at least two semiconductor devices are stacked on each other, and

a conductive line pattern extending from a first electrode on a first major surface of a lower one of said semiconductor devices is connected via a bump to a conductive line pattern extending from a second electrode on a second major surface of an upper one of said semiconductor devices.

26. (New) A composite semiconductor device structure comprising a packaging board having a conductive pattern on a major surface thereof and a plurality of semiconductor devices as defined in claim 21, placed vertically on said major surface of said packing board, wherein each of said conductive member covering said side surface of said semiconductor chip is connected to said conductive pattern on said major surface of said packaging board.